Please replace the paragraph on pg. 13, line 15 - pg. 14, line 2 with the following:

A plurality of dummy trenches 56 may be formed in dielectric layer 50 between a series of relatively narrow trenches 52 and a relatively wide trench 54. While the dimensions of these trenches may vary depending on the design specifications, the dummy trenches 56 are preferably 1 to 5 microns in width, the narrow trenches 52 preferably have sub-micron widths, and the wide trench 54 is preferably greater than 50 microns in width. Also, the depths of all the trenches may range from 2,000 Å to 1 micron. Further, the set of relatively narrow trenches 52 may be spaced apart by a distance of less than 1 micron and from the relatively wide trench 54 by a distance greater than 50 microns. Although the spacing between dummy trenches 56 may vary, this spacing may, e.g., range from 0.5 micron to 50 micron. The trenches may be formed by lithographically patterning a photoresist layer upon dielectric layer 50 to expose select portions of the depicted dielectric. The select portion of dielectric layer 50 not covered by the patterned photoresist is then etched using an etch technique, e.g., a CF_4 plasma etch.

In the Claims:

Please amend claims 1, 9, and 17 to read as follows. A "marked-up" version of these amendments is included in **Attachment A**.

1. (Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said trenches with a conductive material;

polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said narrow and wide trenches, wherein said dummy conductors are electrically separate from of electrically conductive features of an ensuing integrated circuit.

9. (Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive relatively narrow interconnect features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit.

17. (Amended) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said narrow and wide trenches, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

Please add the following claims

21. (Added) The method of claim 1, wherein said dummy conductors are substantially co-planar with said interconnect.

22. (Added) The method of claim 9, wherein said dummy conductors are substantially co-planar with said interconnect.